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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/612,582	NARAHARA ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicant's Amendments, mailed on May 18, 2004. Claims 1, 3, 5-8, 11, 15, 25, 27 and 28 were amended. Claims 29 and 30 were added. Claims 1-30 are pending. This office action is made non-final.

Response to Arguments

2. Applicant's arguments filed on May 18, 2004 with respect to claim rejections under 35 U.S.C. 102 (a) and 103 (a) have been fully considered. New claim rejections under 35 U.S.C. 103 (a) are included in this office action. Examiner's response to Applicant's arguments appears in Paragraph 20 below.

Drawings

3. The drawings submitted on May 18, 2004 are accepted.

Specification

4. The disclosure is objected to because of the following informalities:

Page 3, Lines 24-25, "propagates as a signal waveform, to thereby presents a problem" appears to be incorrect and it appears that it should be "propagates as a signal waveform, to thereby present a problem".

Page 13, Lines 7-9, "The horizontal axis in Fig. 110 represents the time at which change arises in a signal pattern" appears to be incorrect and it appears that it should be "The horizontal axis in Fig. 111 represents the time at which change arises in a signal pattern".

Page 16, Lines 6-9, "the sum of the load-independent and the product of the capacitance information and the load dependent coefficient is taken" appears to be incorrect and it appears that it should be "the sum of the load-independent current and the product of the capacitance information and the load dependent coefficient is taken".

Page 21, Lines 4-5, "calculating a drop in voltage from the amount of electric current flowing in each cell and the resistance of a power" appears to be incorrect and it appears that it should be "calculating a drop in voltage from the amount of electric current flowing in each cell and the resistance of a power line".

Page 23, Lines 10-11, "as the height of the rectangular waveform and the area of the triangular waveform" appears to be incorrect and it appears that it should be "as the height of the rectangular waveform and the area of the rectangular waveform".

Page 25, Lines 21-22, "analysis method as defined in any one of claims 15 through 23, where the calculation step includes" appears to be incorrect and it appears that it should be "analysis method calculation step includes".

Page 26, Lines 4-6, "in consideration of slew information (i.e., an output slew) for an output terminal of a cell for each event information" appears to be incorrect and it appears that it should be "in consideration of slew information (i.e., an output slew) for an output terminal of a cell from each event information".

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 1 is rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential structural cooperative elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are:

electromagnetic interference analyzing step of analyzing the amount of electromagnetic interference arising in an LSI on the basis of a signal output from the FFT processing step.

Such an essential step appears in Claim 28. Without such a step, the electromagnetic analysis method terminates with an FFT processing step and so is incomplete. Additionally, it is not clear as to what is done with the results of FFT analysis.

7. Claim 30 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 30 recites the limitation "The method of claim 28, further comprising the step of providing a gate level simulator". There is insufficient antecedent basis for this limitation in the claim. Claim 28 refers to "An electromagnetic interference analysis system" and not a method and includes "means for" and not steps.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1 and 28 are rejected under 35 U.S.C. 102(a) as being anticipated by **Hayashi et al.** ("EMI- Noise analysis under ASIC design environment", ACM 1999) in view of **Bonitz** (U.S. Patent 6,237,126).

10.1 **Hayashi et al.** teaches EMI Noise analysis under ASIC design environment. Specifically, as per Claim 1, **Hayashi et al.** teaches an electromagnetic interference analysis method for analyzing the amount of electromagnetic interference arising in an LSI by means of performing a logic simulation (Page 16, CL1, Abstract; Page 16, CL2, Para 4; Page 17, CL1, Para 1; Page 18, CL2, Para 4; Page 19, Fig. 12); the method comprising:

an instantaneous current calculation step of calculating the amount of instantaneous electric current from event information, the information being produced when a change arises in a signal (Page 16, CL2, Para 1; Page 16, CL2, Para 3; Page 18, CL2, Para 4; Page 19, CL1, Fig 12; Page 19, CL2, Para 2); and

including the instance name of each cell in which the change has arisen, the name of the signal, a time at which the change has arisen, and transition information (Page 18, CL2, Para 4; Page 19, CL1, Fig 12; Page 19, CL2, Para 2; the event when cell switches is recorded in the logic simulation and the current waveforms of the area obtained; the simulation uses the netlist);

a modeling step of modeling the instantaneous electric current according to a predetermined rule (Page 18, CL2, Para 4 to Page 19, CL1, Para 2; Page 19, Fig. 10); and

an FFT processing step of subjecting to fast Fourier processing the information concerning a change in electric current, the information being calculated through the modeling

step (Page 19, CL2, Para 3; Page 18, CL2, Para 4 to Page 19, CL1, Para 1; Page 16, CL2, Para 3; Page 16, CL2, Para 3).

Hayashi et al. does not expressly teach including the instance name of each cell in which the change has arisen, the name of the signal, a time at which the change has arisen, and transition information (using a logic simulation without netlist). **Bonitz** teaches including the instance name of each cell in which the change has arisen, the name of the signal, a time at which the change has arisen, and transition information (using a logic simulation without netlist) (CL1, L60 to CL2, L6; CL2, L25-40; CL2, 47-50), as cell based simulations result in acceptable computing times for simulation models (CL2, L28-30) and produce good estimates of functional behavior in connection with electromagnetic interference emission of the cells (CL2, L40-46). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Bonitz** that included including the instance name of each cell in which the change has arisen, the name of the signal, a time at which the change has arisen, and transition information (using a logic simulation without netlist), as cell based simulations would result in acceptable computing times for simulation models and would produce good estimates of functional behavior in connection with electromagnetic interference emission of the cells.

10.2 As per Claim 28, **Hayashi et al.** teaches an electromagnetic interference analysis system for analyzing the amount of electromagnetic interference arising in an LSI by means of

performing a logic simulation (Page 16, CL1, Abstract; Page 16, CL2, Para 4; Page 17, CL1, Para 1; Page 18, CL2, Para 4; Page 19, Fig. 12); the system comprising:

a logic simulator (Page 18, CL2, Para 4);

computation means which is connected to the logic simulator and calculates the amount of instantaneous electric current from event information, the information being produced when a change arises in a signal (Page 16, CL2, Para 1; Page 16, CL2, Para 3; Page 18, CL2, Para 4; Page 19, CL1, Fig 12; Page 19, CL2, Para 2); and

including the instance name of each cell in which the change has arisen, the name of the signal, a time at which the change has arisen, and transition information (Page 18, CL2, Para 4; Page 19, CL1, Fig 12; Page 19, CL2, Para 2; the event when cell switches is recorded in the logic simulation and the current waveforms of the area obtained; the simulation uses the netlist);

modeling means for modeling the instantaneous electric current according to a predetermined rule (Page 18, CL2, Para 4 to Page 19, CL1, Para 2; Page 19, Fig. 10); and

fast Fourier (FFT) conversion means for subjecting to fast Fourier processing the information concerning a change in electric current, the information being calculated through the modeling means (Page 19, CL2, Para 3; Page 18, CL2, Para 4 to Page 19, CL1, Para 1; Page 16, CL2, Para 3; Page 16, CL2, Para 3);

thereby analyzing the amount of electromagnetic interference arising in an LSI on the basis of a signal output from the FFT conversion means (Page 19, CL2, Para 3; Page 16, CL2, Para 3; Page 16, CL2, Para 3).

Hayashi et al. does not expressly teach including the instance name of each cell in which the change has arisen, the name of the signal, a time at which the change has arisen, and transition information (using a logic simulation without netlist). **Bonitz** teaches including the instance name of each cell in which the change has arisen, the name of the signal, a time at which the change has arisen, and transition information (using a logic simulation without netlist) (CL1, L60 to CL2, L6; CL2, L25-40; CL2, 47-50), as cell based simulations result in acceptable computing times for simulation models (CL2, L28-30) and produce good estimates of functional behavior in connection with electromagnetic interference emission of the cells (CL2, L40-46). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Bonitz** that included including the instance name of each cell in which the change has arisen, the name of the signal, a time at which the change has arisen, and transition information (using a logic simulation without netlist), as cell based simulations would result in acceptable computing times for simulation models and would produce good estimates of functional behavior in connection with electromagnetic interference emission of the cells.

11. Claims 2, 11, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi et al.** ("EMI- Noise analysis under ASIC design environment", ACM 1999) in view of **Bonitz** (U.S. Patent 6,237,126), and further in view of **Chen et al.** ("Power supply Noise analysis methodology for Deep-submicron VLSI chip design", ACM 1997).

11.1 As per Claim 2, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** teaches that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current (Page 19, CL2, Para 3).

Hayashi et al. does not expressly teach that the modeling step includes an averaging step of averaging the instantaneous current over a certain discrete width; and that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being produced by the averaging step. **Chen et al.** teaches that the modeling step includes an averaging step of averaging the instantaneous current over a certain discrete width (Page 3, CL1, Para 3 to Page 3, CL2, Para 6); and that the FFT processing step includes the information produced by the averaging step (Page 3, CL1, Para 3), as a triangular or trepeziodal current waveform, which is a simpler form of the piecewise linear current model can be derived from the total average current, the piecewise linear current models mimicing the waveforms of the actual circuits (Page 3, CL1, Para 3); and as per **Hayashi et al.**, using the power network and switching current waveform data, SPICE simulation can be performed and current/voltage waveforms obtained; by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Chen et al.** that included the modeling step including an averaging step of averaging the instantaneous current over a certain discrete width; and the FFT processing step including the information produced by the averaging step, as a triangular or trepeziodal current waveform, which would be a simpler form of the piecewise linear current model could be derived from the total average current, the piecewise linear current

models mimicing the waveforms of the actual circuits; that would allow obtaining the switching current waveform as a function of input slew and output load; using the power network and switching current waveform data, SPICE simulation could be performed and current/voltage waveforms obtained; by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

11.2 As per Claim 11, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** teaches that the modeling step includes a triangular waveform modeling step of modeling the instantaneous current as a triangular waveform (Page 19, CL1, Para 1; Fig 10); and that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being calculated in the triangular waveform modeling step (Page 19, CL2, Para 3).

Hayashi et al. does not expressly teach that triangular waveform has a given width and whose height is calculated for each event information such that the amount of instantaneous electric current becomes equal to the area of the triangular waveform. **Chen et al.** teaches that triangular waveform has a given width and whose height is calculated for each event information such that the amount of instantaneous electric current becomes equal to the area of the triangular waveform (Page 3, CL1, Para 3 to Page 3, CL2, Para 6), as a triangular or trepeziodal current waveform, which is a simpler form of the piecewise linear current model can be derived from the total average current, the piecewise linear current models mimicing the waveforms of the actual circuits (Page 3, CL1, Para 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of

Chen et al. that included triangular waveform having a given width and whose height would be calculated for each event information such that the amount of instantaneous electric current became equal to the area of the triangular waveform, as a triangular or trepeziodal current waveform, which would be a simpler form of the piecewise linear current model could be derived from the total average current, the piecewise linear current models mimicing the waveforms of the actual circuits.

11.3 As per Claim 25, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** teaches that the modeling step includes a triangular waveform modeling step of modeling the instantaneous current as a triangular waveform (Page 19, CL1, Para 1; Fig 10) in consideration of slew information (i.e., an output slew) for an output terminal of a cell (Page 18, CL2, Para 4). **HA** teaches that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being calculated in the triangular waveform modeling step (Page 19, CL2, Para 3).

Hayashi et al. does not expressly teach that triangular waveform width is calculated from each event information such that the area of the triangular waveform becomes equal to the amount of electric current of each event, the height of the triangular waveform being calculated on the basis of the width. **Chen et al.** teaches that triangular waveform width is calculated from each event information such that the area of the triangular waveform becomes equal to the amount of electric current of each event, the height of the triangular waveform being calculated on the basis of the width (Page 3, CL1, Para 3 to Page 3, CL2, Para 6), as a triangular or trepeziodal current waveform, which is a simpler form of the piecewise linear current model can

be derived from the total average current, the piecewise linear current models mimicing the waveforms of the actual circuits (Page 3, CL1, Para 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Chen et al.** that included triangular waveform width being calculated from each event information such that the area of the triangular waveform became equal to the amount of electric current of each event, the height of the triangular waveform being calculated on the basis of the width, as a triangular or trepeziodal current waveform, which would be a simpler form of the piecewise linear current model could be derived from the total average current, the piecewise linear current models mimicing the waveforms of the actual circuits.

11.4 As per Claim 26, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** teaches that the modeling step includes means of multiplying the amount of instantaneous electric current by a coefficient corresponding to the state of an event of a cell, in consideration of whether the event of the cell is in a rising state or a falling state (Page 18, CL2, Para 4 to Page 19, CL1, Para 1; Fig 10).

Hayashi et al. does not expressly teach that the modeling step includes a triangular height calculation step of calculating the height of a triangular waveform such that the area of the triangular waveform becomes equal to the amount of electric current of each event. **Chen et al.** teaches that the modeling step includes a triangular height calculation step of calculating the height of a triangular waveform such that the area of the triangular waveform becomes equal to the amount of electric current of each event (Page 3, CL1, Para 3 to Page 3, CL2, Para 6), as a triangular or trepeziodal current waveform, which is a simpler form of the piecewise linear

current model can be derived from the total average current, the piecewise linear current models mimicing the waveforms of the actual circuits (Page 3, CL1, Para 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Chen et al.** that included the modeling step including a triangular height calculation step of calculating the height of a triangular waveform such that the area of the triangular waveform becomes equal to the amount of electric current of each event, as a triangular or trepeziodal current waveform, which would be a simpler form of the piecewise linear current model could be derived from the total average current, the piecewise linear current models mimicing the waveforms of the actual circuits.

12. Claims 3-7, 15-17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi et al.** ("EMI- Noise analysis under ASIC design environment", ACM 1999) in view of **Bonitz** (U.S. Patent 6,237,126), and further in view of **Roethig** (U.S. Patent 5,835,380).

12.1 As per Claim 3, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** teaches that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being calculated in the rectangular waveform modeling step (Page 19, CL2, Para 3).

Hayashi et al. does not expressly teach that the modeling step includes a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform whose height is calculated from information for each event such that the area of the rectangular waveform becomes equal to the amount of electric current of each event. **Roethig** teaches that

the modeling step includes a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform whose height is calculated from information for each event such that the area of the rectangular waveform becomes equal to the amount of electric current of each event (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22), because rectangular waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included the modeling step including a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform whose height was calculated from information for each event such that the area of the rectangular waveform became equal to the amount of electric current of each event; and the FFT processing step including the information calculated in the rectangular waveform modeling step, as rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

12.2 As per Claim 4, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** teaches that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being calculated in the geometrically-similar rectangular waveform modeling step (Page 19, CL2, Para 3).

Hayashi et al. does not expressly teach that the modeling step includes a rectangular waveform modeling step of modeling the instantaneous current as a geometrically-similar rectangular waveform whose height is calculated from information for each event such that the area of the rectangular waveform becomes equal to the amount of electric current of each event. **Roethig** teaches that the modeling step includes a rectangular waveform modeling step of modeling the instantaneous current as a geometrically-similar rectangular waveform whose height is calculated from information for each event such that the area of the rectangular waveform becomes equal to the amount of electric current of each event (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22), because rectangular waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included the modeling step including a rectangular waveform modeling step of modeling the instantaneous current as a geometrically-similar rectangular waveform whose height was calculated from information for

each event such that the area of the rectangular waveform became equal to the amount of electric current of each event; and the FFT processing step including the information calculated in the rectangular waveform modeling step, as rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

12.3 As per Claim 5, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** teaches subjecting to FFT processing the information concerning a change in electric current calculated in the rectangular waveform modeling step (Page 19, CL2, Para 3)

Hayashi et al. does not expressly teach that the modeling step includes a rectangular waveform modeling step of calculating the instantaneous electric current from each event information, and a step of modeling the instantaneous current as a rectangular waveform through use of the amount of electric current and a table representing the relationship between the width and height of a rectangular waveform. **Roethig** teaches that the modeling step includes a rectangular waveform modeling step of calculating the instantaneous electric current from each event information, and a step of modeling the instantaneous current as a rectangular waveform through use of the amount of electric current and a table representing the relationship between the width and height of a rectangular waveform (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22; CL3, L23-25), because rectangular waveforms represent the Vdd and Vss

currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included the modeling step including a rectangular waveform modeling step of calculating the instantaneous electric current from each event information, and a step of modeling the instantaneous current as a rectangular waveform through use of the amount of electric current; and subjecting to FFT processing the information concerning a change in electric current calculated in the rectangular waveform modeling step, as rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

12.4 As per Claim 6, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** teaches the modeling step includes a step of calculating the instantaneous electric current from information for each event (Page 16, CL2, Para 1; Page 16, CL2, Para 3; Page 18, CL2, Para 4; Page 19, CL1, Fig 12; Page 19, CL2, Para 2); and a modeling step of modeling the instantaneous current through use of a slew in input waveform (Page 18, CL2, Para 4), to thereby subject to

FFT processing the information concerning a change in electric current calculated in the rectangular waveform modeling step (Page 19, CL2, Para 3)

Hayashi et al. does not expressly teach a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform through use of a table representing the relationship between the width and height of a rectangular waveform. **Roethig** teaches a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform through use of a table representing the relationship between the width and height of a rectangular waveform (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22; CL3, L23-25), because rectangular waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform through use of a table representing the relationship between the width and height of a rectangular waveform, as rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of

the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

12.5 As per Claim 7, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** teaches the modeling step includes a step of calculating the instantaneous electric current from information for each event (Page 16, CL2, Para 1; Page 16, CL2, Para 3; Page 18, CL2, Para 4; Page 19, CL1, Fig 12; Page 19, CL2, Para 2); and a modeling step of modeling the instantaneous current through use of an output load capacitance (Page 18, CL2, Para 4), to thereby subject to FFT processing the information concerning a change in electric current calculated in the rectangular waveform modeling step (Page 19, CL2, Para 3)

Hayashi et al. does not expressly teach a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform through use of a table representing the relationship between the width and height of a rectangular waveform. **Roethig** teaches a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform through use of a table representing the relationship between the width and height of a rectangular waveform (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22; CL3, L23-25), because rectangular waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one

of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform through use of a table representing the relationship between the width and height of a rectangular waveform, as rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

12.6 As per Claim 15, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** teaches that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being calculated in the rectangular waveform modeling step (Page 19, CL2, Para 3).

Hayashi et al. does not expressly teach that the modeling step includes a calculation step of calculating the height of a rectangular waveform from a library in which peak currents of cells are characterized according to the type of cell, and a rectangular waveform modeling step of modeling the amount of instantaneous electric current as a rectangular waveform, the peak current calculated in the calculation step being taken as the height of the rectangular waveform and the area of the rectangular waveform being equal to the amount of electric current of each event. **Roethig** teaches that the modeling step includes a calculation step of calculating the height of a rectangular waveform from a library in which peak currents of cells are characterized

according to the type of cell, and a rectangular waveform modeling step of modeling the amount of instantaneous electric current as a rectangular waveform, the peak current calculated in the calculation step being taken as the height of the rectangular waveform and the area of the rectangular waveform being equal to the amount of electric current of each event (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22; CL3, L23-25), because rectangular waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included the modeling step including a calculation step of calculating the height of a rectangular waveform from a library in which peak currents of cells were characterized according to the type of cell, and a rectangular waveform modeling step of modeling the amount of instantaneous electric current as a rectangular waveform, the peak current calculated in the calculation step being taken as the height of the rectangular waveform and the area of the rectangular waveform being equal to the amount of electric current of each event, as rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load

current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

12.7 As per Claim 16, **Hayashi et al., Bonitz** and **Roethig** teach the method of claim 15. **Hayashi et al.** also teaches that the calculation step includes a step of calculating a peak current for each cell from information concerning a slew in the cell, by reference to a library in which the relationship between a slew in input waveform and a peak current is characterized in the form of a table according to the type of cell (Page 18, CL2, Para 4).

12.8 As per Claim 17, **Hayashi et al., Bonitz** and **Roethig** teach the method of claim 15. **Hayashi et al.** also teaches that the calculation step includes a step of calculating a peak current for each cell from information concerning a load capacitance of a cell, by reference to a library in which the relationship between a load capacitance and a peak current is characterized in the form of a table according to the type of cell (Page 18, CL2, Para 4).

12.9 As per Claim 20, **Hayashi et al., Bonitz** and **Roethig** teach the method of claim 15. **Hayashi et al.** does not expressly teach that the calculation step includes a step of calculating the height of a rectangular waveform through use of a library in which peak currents are characterized in consideration of the state of an input signal. **Roethig** teaches that the calculation step includes a step of calculating the height of a rectangular waveform through use of a library in which peak currents are characterized in consideration of the state of an input signal (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22; CL3, L23-25), because rectangular

waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included the calculation step including a step of calculating the height of a rectangular waveform through use of a library in which peak currents were characterized in consideration of the state of an input signal, as rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

13. Claims 8-10 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi et al.** ("EMI- Noise analysis under ASIC design environment", ACM 1999) in view of **Bonitz** (U.S. Patent 6,237,126), and further in view of **Kuwano et al.** (U.S. Patent 6,253,354).

13.1 As per Claim 8, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** teaches that the modeling step includes the resistance of a power line and correcting the amount of instantaneous electric current of each cell for each event, on the basis of the relationship

between the drop in voltage and the amount of instantaneous electric current (Page 19, CL1, Para 2; Page 18, CL1, Para 6 to CL2, Para 1).

Hayashi et al. does not expressly teach calculating a drop in voltage from the amount of electric current flowing in each cell and the resistance of a power line. **Kuwano et al.** teaches calculating a drop in voltage from the amount of electric current flowing in each cell and the resistance of a power line (CL2, L29-33), as that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns (CL1, L9-10). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Kuwano et al.** that included calculating a drop in voltage from the amount of electric current flowing in each cell and the resistance of a power line, as that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns.

13.2 As per Claim 9, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** teaches that the modeling step includes the resistance of a power line, and the capacitance of an on-chip capacitor and correcting the amount of instantaneous electric current of each cell for each event, on the basis of the relationship between the drop in voltage and the amount of instantaneous electric current (Page 19, CL1, Para 2; Page 17, CL1, Para 3 to Page 18, CL2, Para 1; Page 16, CL2, Para 8; Page 18, CL2, Fig 8).

Hayashi et al. does not expressly teach calculating a drop in voltage from the amount of electric current flowing in each cell and the resistance of a power line, and the capacitance of an on-chip capacitor. **Kuwano et al.** teaches calculating a drop in voltage from the amount of

electric current flowing in each cell and the resistance of a power line, and the capacitance of an on-chip capacitor (CL2, L29-33), as that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns (CL1, L9-10). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Kuwano et al.** that included calculating a drop in voltage from the amount of electric current flowing in each cell and the resistance of a power line, and the capacitance of an on-chip capacitor, as that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns.

13.3 As per Claim 10, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** teaches that the modeling step includes a step of transiently analyzing a power RC of each cell and a cell power source, and a correction step of correcting the amount of instantaneous electric current of each cell for each event, on the basis of the relationship between the drop in voltage and the amount of instantaneous electric current (Page 19, CL1, Para 2; Page 17, CL1, Para 3 to Page 18, CL2, Para 1; Page 16, CL2, Para 8; Page 18, CL2, Fig 8).

Hayashi et al. does not expressly teach accurately calculating a drop in voltage. **Kuwano et al.** teaches accurately calculating a drop in voltage (CL2, L29-33), as that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns (CL1, L9-10). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Kuwano et al.** that included accurately calculating a drop in voltage, as that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns.

13.4 As per Claim 23, **Hayashi et al., Bonitz** and **Kuwano et al.** teach the method of claim 10. **Hayashi et al.** teaches that the correction step includes a step of iterating several times calculation of a drop in voltage and correction of a current waveform (Page 19, CL1, Para 3).

14. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi et al.** ("EMI- Noise analysis under ASIC design environment", ACM 1999) in view of **Bonitz** (U.S. Patent 6,237,126), and further in view of **Schaefer** (U.S. Patent 5,617,325).

14.1 As per Claim 12, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** teaches that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being calculated in the multi-order-function waveform modeling step (Page 19, CL2, Para 3)

Hayashi et al. does not expressly teach that the modeling step includes a multi-order-function waveform modeling step of modeling the instantaneous current as a multi-order-function waveform. **Schaefer** teaches that the modeling step includes a multi-order-function waveform modeling step of modeling the instantaneous current as a multi-order-function waveform (CL6, L2-13) because the step response of a target element can be represented by a multi-order-function, when a voltage step from an initial voltage to a final voltage is applied to the input node of an element (CL6, L5-13). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Schaefer** that included the modeling step including a

multi-order-function waveform modeling step of modeling the instantaneous current as a multi-order-function waveform, as the step response of a target element could be represented by a multi-order-function, when a voltage step from an initial voltage to a final voltage is applied to the input node of an element.

14.2 As per Claim 13, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** teaches that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being calculated in the exponential-function waveform modeling step (Page 19, CL2, Para 3)

Hayashi et al. does not expressly teach that the modeling step includes an exponential function waveform modeling step of modeling the instantaneous current as an exponential-function waveform. **Schaefer** teaches that the modeling step includes an exponential function waveform modeling step of modeling the instantaneous current as an exponential-function waveform (Fig. 5; CL5, L42-52), because the exponential waveform models the current that approaches asymptotically the final value as the voltage approaches asymptotically the final value (CL5, 49-50). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Schaefer** that included the modeling step including an exponential function waveform modeling step of modeling the instantaneous current as an exponential-function waveform, because the exponential waveform would model the current that approaching asymptotically the final value as the voltage approached asymptotically the final value.

15. Claims 14, 29 and 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi et al.** ("EMI- Noise analysis under ASIC design environment", ACM 1999) in view of **Bonitz** (U.S. Patent 6,237,126), and further in view of **Zarkesh et al.** (U.S. Patent 6,212,665).

15.1 As per Claim 14, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** does not expressly teach that the modeling step includes a step of modeling the amount of instantaneous electric current while separating the same into a short circuit electric current component and a charge current component. **Zarkesh et al.** teaches that the modeling step includes a step of modeling the amount of instantaneous electric current while separating the same into a short circuit electric current component and a charge current component (Abstract, L1-5 and L11-19; Fig. 5E; CL2, L59-64; CL7, L1-8), as the energy dissipation caused by switching activity is a function of charge /discharge current and short circuit current for a given cell of specified characteristics (CL7, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Zarkesh et al.** that included the modeling step including a step of modeling the amount of instantaneous electric current while separating the same into a short circuit electric current component and a charge current component, as the energy dissipation caused by switching activity would be a function of charge /discharge current and short circuit current for a given cell of specified characteristics.

15.2 As per Claim 29, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** does not expressly teach the method further comprising the step of providing a gate level logic

simulation. **Bonitz** teaches the method further comprising the step of providing a gate level logic simulation (CL1, L60 to CL2, L6; CL2, L25-40; CL2, 47-50), as cell based simulations result in acceptable computing times for simulation models (CL2, L28-30) and produce good estimates of functional behavior in connection with electromagnetic interference emission of the cells (CL2, L40-46); and as per **Zarkesh et al.** a cell simulator includes a gate level simulator, since a cell could be a gate (CL1, L40-47). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Bonitz** that included the method further comprising the step of providing a gate level logic simulation, as cell based simulations would result in acceptable computing times for simulation models and would produce good estimates of functional behavior in connection with electromagnetic interference emission of the cells; and a cell simulator would include a gate level simulator, since a cell could be a gate.

15.3 As per Claim 30, **Hayashi et al.** and **Bonitz** teach the system of claim 28. **Hayashi et al.** does not expressly teach the step of providing a gate level logic simulator. **Bonitz** the step of providing a gate level logic simulator (CL1, L60 to CL2, L6; CL2, L25-40; CL2, 47-50), as cell based simulations result in acceptable computing times for simulation models (CL2, L28-30) and produce good estimates of functional behavior in connection with electromagnetic interference emission of the cells (CL2, L40-46); and as per **Zarkesh et al.** a cell simulator includes a gate level simulator, since a cell could be a gate (CL1, L40-47). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Bonitz** that included the step of providing a gate level logic simulator, as

cell based simulations would result in acceptable computing times for simulation models and would produce good estimates of functional behavior in connection with electromagnetic interference emission of the cells; and a cell simulator would include a gate level simulator, since a cell could be a gate.

16. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi et al.** ("EMI- Noise analysis under ASIC design environment", ACM 1999) in view of **Bonitz** (U.S. Patent 6,237,126), and further in view of **Roethig** (U.S. Patent 5,835,380) and **Kamiya et al.** (U.S. Patent 6,304,998).

16.1 As per Claim 18, **Hayashi et al., Bonitz** and **Roethig** teach the method of claim 15. **Hayashi et al.** does not expressly teach that the calculation step includes a step of setting a plurality of peak currents for a composite cell. **Kamiya et al.** teaches that the calculation step includes a step of setting a plurality of peak currents for a composite cell (Abstract, L1-10; Fig 13; Fig. 31 and 32; CL1, L19-23), because the instantaneous current for the composite cells (macros) comprising a plurality of cells varies depending on the input through rate of the input signal supplied to the input terminal and the load capacitance connected to the output terminal (CL2, L8-12). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Kamiya et al.** that included the calculation step including a step of setting a plurality of peak currents for a composite cell, because the instantaneous current for the composite cells (macros) comprising a

plurality of cells would vary depending on the input through rate of the input signal supplied to the input terminal and the load capacitance connected to the output terminal.

Hayashi et al. does not expressly teach that calculating the heights of a plurality of rectangular waveforms through use of a characterized library, and the rectangular waveform modeling step corresponds to a step of modeling the amount of electric current into a plurality of rectangular waveforms. **Roethig** teaches that calculating the heights of a plurality of rectangular waveforms through use of a characterized library, and the rectangular waveform modeling step corresponds to a step of modeling the amount of electric current into a plurality of rectangular waveforms (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22; CL3, L23-25), because rectangular waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included calculating the heights of a plurality of rectangular waveforms through use of a characterized library, and the rectangular waveform modeling step corresponding to a step of modeling the amount of electric current into a plurality of rectangular waveforms, as rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by

changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

16.2 As per Claim 19, **Hayashi et al., Bonitz** and **Roethig** teach the method of claim 15. **Hayashi et al.** does not expressly teach that the calculation step includes a step of setting a plurality of peak currents for each of the rise and fall of a flip-flop (FF) cell. **Kamiya et al.** teaches that the calculation step includes a step of setting a plurality of peak currents for each of the rise and fall of a flip-flop (FF) cell (Abstract, L1-10; Fig 13; Fig. 31 and 32; CL1, L19-23), because the instantaneous current for the composite cells (macros) comprising a plurality of cells varies depending on the input through rate of the input signal supplied to the input terminal and the load capacitance connected to the output terminal (CL2, L8-12). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Kamiya et al.** that included the calculation step including a step of setting a plurality of peak currents for each of the rise and fall of a flip-flop (FF) cell, because the instantaneous current for the composite cells (macros) comprising a plurality of cells would vary depending on the input through rate of the input signal supplied to the input terminal and the load capacitance connected to the output terminal.

Hayashi et al. does not expressly teach that calculating the heights of a plurality of rectangular waveforms through use of a characterized library, and the rectangular waveform modeling step corresponds to a step of modeling the amount of electric current into a plurality of rectangular waveforms. **Roethig** teaches that calculating the heights of a plurality of rectangular waveforms through use of a characterized library, and the rectangular waveform modeling step

corresponds to a step of modeling the amount of electric current into a plurality of rectangular waveforms (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22; CL3, L23-25), because rectangular waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included calculating the heights of a plurality of rectangular waveforms through use of a characterized library, and the rectangular waveform modeling step corresponding to a step of modeling the amount of electric current into a plurality of rectangular waveforms, as rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

17. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi et al.** ("EMI- Noise analysis under ASIC design environment", ACM 1999) in view of **Bonitz** (U.S. Patent 6,237,126), and further in view of **Roethig** (U.S. Patent 5,835,380), and **Kuwano et al.** (U.S. Patent 6,253,354).

17.1 As per Claim 21, **Hayashi et al., Bonitz** and **Roethig** teach the method of claim 15. **Hayashi et al.** teaches a correction step of characterizing, for each cell, the relationship between a drop in voltage and the amount of instantaneous electric current in the form of a table, to thereby correct the amount of instantaneous electric current for each event of the cell (Page 19, CL1, Para 2).

Hayashi et al. does not expressly teach a step of calculating a drop in voltage from the amount of electric current determined according to the type of cell and from the resistance of a power line. **Kuwano et al.** teaches a step of calculating a drop in voltage from the amount of electric current determined according to the type of cell and from the resistance of a power line (CL2, L29-33), as that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns (CL1, L9-10). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Kuwano et al.** that included a step of calculating a drop in voltage from the amount of electric current determined according to the type of cell and from the resistance of a power line, as that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns.

17.2 As per Claim 22, **Hayashi et al., Bonitz** and **Roethig** teach the method of claim 15. **Hayashi et al.** teaches a correction step of characterizing, for each cell, the relationship between a drop in voltage and the amount of instantaneous electric current in the form of a table, to

thereby correct the amount of instantaneous electric current for each event of the cell (Page 19, CL1, Para 2).

Hayashi et al. does not expressly teach a step of calculating a drop in voltage from the amount of electric current determined according to the type of cell, the resistance of a power line, and the capacitance of an on-chip capacitor. **Kuwano et al.** teaches a step of calculating a drop in voltage from the amount of electric current determined according to the type of cell, the resistance of a power line, and the capacitance of an on-chip capacitor (CL2, L29-33), as that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns (CL1, L9-10). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Kuwano et al.** that included a step of calculating a drop in voltage from the amount of electric current determined according to the type of cell, the resistance of a power line, and the capacitance of an on-chip capacitor, as that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns.

18. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi et al.** ("EMI- Noise analysis under ASIC design environment", ACM 1999) in view of **Bonitz** (U.S. Patent 6,237,126), and further in view of **Roethig** (U.S. Patent 5,835,380), and **Zarkesh et al.** (U.S. Patent 6,212,665).

18.1 **Hayashi et al., Bonitz** and **Roethig** teach the method of claim 15. **Hayashi et al.** does not expressly teach that the calculation step includes a step of modeling the amount of

instantaneous electric current while separating the same into a short circuit electric current component and a charge current component. **Zarkesh et al.** teaches that the calculation step includes a step of modeling the amount of instantaneous electric current while separating the same into a short circuit electric current component and a charge current component (Abstract, L1-5 and L11-19; Fig. 5E; CL2, L59-64; CL7, L1-8), as the energy dissipation caused by switching activity is a function of charge /discharge current and short circuit current for a given cell of specified characteristics (CL7, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Zarkesh et al.** that included the calculation step including a step of modeling the amount of instantaneous electric current while separating the same into a short circuit electric current component and a charge current component, as the energy dissipation caused by switching activity would be a function of charge /discharge current and short circuit current for a given cell of specified characteristics.

19. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi et al.** ("EMI- Noise analysis under ASIC design environment", ACM 1999) in view of **Bonitz** (U.S. Patent 6,237,126), and further in view of **Kamiya et al.** (U.S. Patent 6,304,998).

19.1 As per Claim 27, **Hayashi et al.** and **Bonitz** teach the method of claim 1. **Hayashi et al.** teaches a triangular waveform modeling step of modeling the amount of instantaneous electric current as a plurality of triangular waveforms through use of a table representing the relationship between the width and height of a triangular waveform (Page 19, CL1, Para 1; Fig 10; Page 18,

CL2, Para 4); and the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being calculated in the triangular waveform modeling step (Page 19, CL2, Para 3).

Hayashi et al. does not expressly teach that the modeling step includes a step of calculating the amount of instantaneous electric current from each event information in the case of a composite cell. **Kamiya et al.** teaches that the modeling step includes a step of calculating the amount of instantaneous electric current from each event information in the case of a composite cell (Abstract, L1-10; Fig 13; Fig. 31 and 32; CL1, L19-23), because the instantaneous current for the composite cells (macros) comprising a plurality of cells varies depending on the input through rate of the input signal supplied to the input terminal and the load capacitance connected to the output terminal (CL2, L8-12). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Kamiya et al.** that included the modeling step including a step of calculating the amount of instantaneous electric current from each event information in the case of a composite cell, because the instantaneous current for the composite cells (macros) comprising a plurality of cells would vary depending on the input through rate of the input signal supplied to the input terminal and the load capacitance connected to the output terminal.

Arguments

20. As per the applicant's arguments, the applicants' attention is requested to the corresponding claim rejections. In addition, the following explanation is provided to further explain the examiner's position.

20.1 As per the Applicant's argument that "the applicant does not understand the rejection of claim 1 as incomplete", Applicants' attention is directed to Paragraph 6, which provides the explanation.

20.2 As per the applicant's argument that "**Hayashi** teaches only a simplification model for an electronic source mesh; claims 1 and 28 recite calculating the amount of instantaneous current using gate level current analysis method and modeling the current waveform corresponding to the amount of instantaneous electric current; **Hyashi** proposes realization at the transistor level; the reference merely states the potential of gate-level simulation ... It teaches only an EMS noise analysis system carried out at transistor level ... It does not enable a gate level analysis method .. **Hayashi** does not make it possible to study the effects caused by LSI currents in the frequency domain; **Hayashi** requires parallel use of transistor level and gate level simulation ", the examiner respectfully disagrees.

Hayashi teaches logic simulation using cell switching current waveform library Page 18, CL2, Para 4). The cell simulation includes gate level simulation, since as per **Zarkesh et al.** a cell simulator includes a gate level simulator, since a cell could be a gate (CL1, L40-47). **Hayashi** makes it possible to study the effects caused by LSI currents in the frequency domain (Page 19, CL2, Para 3; FFT transformation permits to study the effects caused by LSI currents in

the frequency domain). In addition, the examiner has used **Bonitz** as additional reference; Bonitz teaches cell based simulation to provide current patterns at all nodes. **Bonitz** teaches including the instance name of each cell in which the change has arisen, the name of the signal, a time at which the change has arisen, and transition information (using a logic simulation without netlist) (CL1, L60 to CL2, L6; CL2, L25-40; CL2, 47-50). **Bonitz** teaches current value changes with respect to time (CL11, L10-18; CL2, L14-15). **Kuwano et al.** also teaches cell based simulation, determining instantaneous currents and calculating maximum current (Fig 9, Fig 10; CL2, L21-27; Cl3, L56-63).

20.3 As per the Applicant's argument that "Hayashi does not specify how the triangular waveform is applied to an event", the examiner has used **Chen** which uses the triangular waveform to calculate the peak current from the instantaneous current obtained in simulation events and the switching activities (Page 3, CL1, Para 3 to Page 3, CL2, Para 6; page 3, CL1, Para 2).

20.4 As per the Applicant's argument that "**Chen** does not suggest electromagnetic interference analysis method; it is concerned with noise generated by an LSI power supply", the examiner has used **Chen** only to show that he uses the triangular waveform to calculate the peak current from the instantaneous current obtained in simulation events and the switching activities (Page 3, CL1, Para 3 to Page 3, CL2, Para 6; page 3, CL1, Para 2).

20.5 As per the Applicant's argument that "the Examiner has not provided proper motivation for adding the averaging function to Hayashi", the examiner has shown **Chen** uses the averaging function to calculate the peak current and the height and width of the waveform (Page 3, CL1, Para 3 to Page 3, CL2, Para 6; page 3, CL1, Para 2). **Kuwano et al.** shows calculation of average current to determine if the power source wiring can secure the current density (CL1, L29-33). The examiner takes the position that the motivation used by others need not be same as the motivation used by the applicants.

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
July 20, 2004

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER